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# A robust 12T SRAM cell with improved write margin for ultra-low power applications in 40 nm CMOS☆

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ABSTRACT

Near-threshold operation is garnering growing attention for ultra-low power applications despite the fact the reliability of the near-threshold digital systems warrants unprecedented scrutiny of robustness measures to ensure correct functionality under stringent environmental and manufacturing scattering specifications. In this paper, an ideal theoretical read and write static noise margins (RSNM/WSNM) are discussed. In addition, a 12T SRAM bit cell is proposed in order to reach the theoretical WSNM limit. This could be achieved by eliminating a feedback of back-to-back inverters by means of data-dependent supply cutoff during write operation. This allows the proposed bit cell to enlarge write margin dramatically. Many previous works also attempt to cutoff the supply, but many of them were not data dependent. Monte-Carlo (MC) simulation results show the proposed 12T SRAM bit cell is more robust in static and dynamic noise margin than the conventional 6T and 8T SRAM bit cells as well as a 10T bit cell. The area overhead of the proposed bit cell is 1.96 times and 1.74 times greater than the 6T and 8T bit cells, respectively. Analytical models of WSNM for the 12T bit cell in the super-threshold region and the sub-threshold region are also proposed.

## 1. Introduction

WITH the advancement of CMOS VLSI technology in nanometer regime, the process, the supply voltage, and the on-chip temperature (PVT) variations have been significant issues. These variations make a digital CMOS system vulnerable since drivability of each device changes from the intended design, causing read or write upset in an SRAM, synchronization problems in a latch, and adversely affect delays in logic gates. Among these three 'canonical' CMOS circuit types which are an SRAM cell, a latch, and an inverter, an SRAM bit cell is a key component in designing a reliable system due to its highest failure rate [1]. In addition, as the demand for ultra-low power applications has been on the rise [2–5], many techniques have been proposed, including parallel computation [6], clock gating [7], low swing signaling [8], dynamic voltage and frequency scaling (DVFS) [9], low swing flops and latches [10], and sub-threshold operation [4]. Among these techniques, sub-threshold operation has had a high profile since dynamic power can dramatically be reduced in the sub-threshold region. In this region, sequential logic is more vulnerable to noise than combinational logic, so many sub-threshold SRAM cell structures have been proposed since the introduction of the first sub-threshold operating FFT processor [4].

A singled-ended read port was proposed by introducing two additional read transistors [11]. These additional devices decouple its read bit line from the storage node, so the disturbance of the SRAM cell can be eliminated during read operation, which improved the stability of SRAM cell during read operation. This proposed bit cell is widely used in [12–15]. Another attempt to reduce read disturbance was introduced in [16]. An additional device is added to the conventional 6T cell so that a pull-down network can be cut from the storage node. However, this approach has drawback for write operation. In another example, the number of read access transistors was increased to four [17]. The additional devices could increase the number of rows sharing a bit line due to stacking effects. In [14], a floating VDD scheme was proposed. In this work, write operation in the sub-threshold region was feasible due to a floating VDD during write operation since it weakened the feedback in the SRAM cell. In addition, a virtual ground concept driven by a read buffer foot driver was introduced, which helped leakage reduction from bit lines through read access devices. For realization of write operation in the sub-threshold region, a virtual supply scheme was introduced. In [18], a decoupled read port was also introduced in order to improve read static noise margin (RSNM), and halo doping was introduced in the access transistors in order to utilize

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reverse short channel effect, causing the increase of threshold voltage. This technique was for increasing write margin in the sub-threshold region. Another approach for improvement of RSNM was proposed in [19]. Dynamic differential cascade voltage switch logic (DCVSL) was introduced for read access. In order to increase write margin, wordline voltage was boosted. Although these proposed bit cells improved RSNM as well as the number of rows sharing a bit line, write margin was not dramatically improved since each bit cell itself has a feedback loop in the structure so that this loop contends with write access devices. Other than the above mentioned bit cells, many proposed SRAM cells drastically improved read stability in the sub-threshold region, but write stability was not improved much [20–23]. Another bit cell was proposed to resolve this issue [24]. In this proposed cell, feedback loop is opened by cutting a pull-down network of a half-cell. However, every bit cell dynamically shares switch control signal during both write and read operations. As a result, the storage nodes might experience voltage droop due to the control signals shared with the other bit cells in a column. Thus, it is potentially hazardous to a dynamic noise source although it suggests a way to improve write margin of SRAM bit cell. In conclusion, no bit cell can be regarded robust enough during write operation in the sub-threshold region. At last, another bit cell is proposed in [25]. The proposed cell cuts the power supply by the data written within the bit cell. However, the supply cutoff can be achieved after the access transistor successfully writes data into a storage node. Thus, the supply cutoff is indirectly controlled through the access transistor. In [26], a single write port bitcell was proposed. During write operation, the power supply to one of the hald cells was cut so that writability was improved. This bitcell structure resembles a standard cell latch, but since the power cutoff is recovered after the write clock cycle, the data is latched after the current clock cycle, which has a potential hazard of noise interference during the clock transition. Another attempt to improve writability of SRAM was proposed in [27]. In this proposed bit cell, pull-up networks are cut to eliminate charge contention during write operation. However, this bit cell also sacrifices hold due to its structure.

Theoretically, the maximum achievable static noise margin can be considered as shown in Fig. 1. Two conventional static noise margins for read (i.e. RSNM) and write (i.e. WSNM) are presented. These ideal margins can be acquired by combining two ideal voltage transfer characteristics (VTCs) of back-to-back inverters. These VTCs depend on each operation. When reading, ideal inverters should switch at $V_M$=VDD/2 with gain=−∞, so when these inverters are connected back-to-back, the DC responses can be represented as in Fig. 1(a). Hence, the maximum RSNM can be VDD/2 from the definition. When writing, the VTC of an inverter is identical to the normal VTC, while the VTC of the other is distorted so that mono-stability condition is met during writing. In order to achieve the ideal mono-stability, one of the VTCs should be the ideal VTC of an inverter, while the other should be a straight line along with y-axis so that those cannot intersect (i.e. hold a state) with each other. As shown in Fig. 1(b), the maximum WSNM can be VDD/2. This point of view presents a blueprint on how the static noise margin of an ideal SRAM would be.

In this paper, a 12T SRAM cell is proposed, which eliminates charge contention during write operation so that its VTC curves closely resemble the ideal VTC curves for WSNM. Therefore, the proposed bit cell is bulletproof as a bit cell design can be even in the sub-threshold region where device performance variation is extremely difficult to manage. As mentioned in the following chapters, the proposed cell work at some frequency no matter how the devices are sized. The only significant considerations that affect device sizing are performance (i.e. speed and power).

The proposed bit cell can be used in ultra-low power applications (i.e. sub-threshold operation) since reliability is a concern in the sub-threshold region. In many cases, these applications require a small capacity of memory so that the size overhead of a bit cell might not be critical, compared to memory hungry applications. If the bit cell cannot find a way into production due to the size overhead, it might at least serve as the 'pseudo-golden reference' for all subthreshold bit cell designs to be compared against since the proposed bit cell is as safe as a bit cell could ever be in terms of read and write static noise margin. Although a standard-cell latch proposed in [28] can be regarded as a golden reference due to no charge contention, the voltage transfer characteristic of the proposed 12T bitcell is also similar to the one of the standard-cell latch. The difference between them is that the proposed bitcell has initial charge contention, while the standard cell latch does not have any charge contention. However, the proposed bitcell forms a feedback loop during the write operation clock phase, while the standard cell latch forms it after the write operation clock phase. Since the characteristics of the proposed bitcell is very similar to the standard cell latch, the other sub-threshold bit cells traded safety and robustness for area reduction, so the degree to which it is accomplished could be compared to the proposed bit cell as a reference.

The proposed bit cell structure is based on a 16T SRAM proposed in [29]. While the 16T bit cell has dual-rail outputs and two footers for balancing the signal timing of dual-rail in asynchronous systems, the proposed 12 T SRAM bit cell has a single-ended output and no footer to reduce area and power overhead.

The remainder of this paper is organized as follows: Section 2 describes the proposed 12T SRAM bit cell design, its operation principle, and sizing constraint. Section 3 introduces sub-threshold and super-threshold analytical models for the write margin of the proposed 12T SRAM. Section 4 presents simulation results. Section 5 draws conclusions.

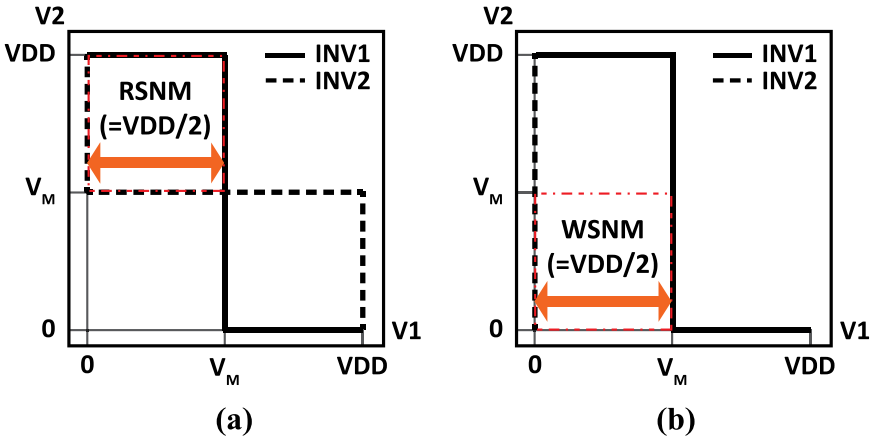


**Fig. 1.** Ideal noise margin curves for (a) RSNM and (b) WSNM.

## 2. 12T SRAM cell design

12T SRAM is designed to increase write margin. Previously proposed SRAM cells are mostly either for improving read static noise margin or for increasing the number of rows SRAM cells share in bit lines by reducing leakage current. Consequently, not many attempts to increase write margin have been done.

Conventionally, write operation is conducted by applying state '0' or '1' to the bit lines so that the set values can override the previous state stored in the cross-coupled inverters. In this scenario, bit line input drivers should be stronger than SRAM cell transistors, otherwise, write operation may fail. Due to this characteristic of an SRAM, sizing has been one of the most dominant factors for designing an SRAM cell. This is attributed to SRAM cell's feedback loop structure—back-to-back inverter structure. In an instance of read operation, the read access switches can be used for decoupling the read bit lines from the storage nodes as an 8T SRAM cell, so these read access transistors can be free from sizing constraints. In the case of write operation, however, decoupling storage nodes from bit lines is infeasible because some paths through which charges can be stored or discharged should directly be connected to those nodes. Accordingly, an alternative bitcell needs to be proposed such as a static logic style.

### 2.1. SRAM cell structure

The proposed SRAM cell structure is shown in Fig. 2. Storage nodes Q and QB are comprised of transistors M1 through M4. More specifically, transistors M1 through M4 are arranged as a pair of inverters cross-coupled with each other. Transistors M7 through M10 comprise supply switches defined as two pairs of PMOS devices, such that each pair of PMOS devices have source terminals coupled to the supply voltage and drain terminals coupled to one of the two inverters. Additionally, a gate terminal of a single supply transistor is coupled to a write word line. Write access switches are comprised of transistors M5 and M6 as the conventional 6T and 8T SRAM cells are. These six devices—M5 through M10—relate write operation. Two NMOS devices M11 and M12 form a read port as in the conventional 8T SRAM cell [11].

### 2.2. Operation principle

12T SRAM is fully operated in static mode during read and write operation.

#### 2.2.1. Read operation

Read operation is conducted through devices M11 and M12 as shown in Fig. 3. As in a conventional 8T SRAM cell, the storage node QB is decoupled from the read bit lines RBL by device M11. In this case, M11 is turned on. When RWL is asserted, a path from RBL to VGND becomes transparent, and VGND is driven to GND by a driver, as shown in Fig. 3(a). Once this path is transparent, charges on the floating bit line, RBL, begin to be discharged through the path as shown in Fig. 3(b). This process is the completion of read operation. After this completion, RWL is deasserted and RBL is precharged to VDD, while VGND is driven to VDD so that the leakage due to lack of voltage difference between RBL and VGND can be reduced when the SRAM cells connected to this word line are not used. It brings about more rows of cells shared in bit lines since the leakage has been an obstacle increasing the number of rows of cells.

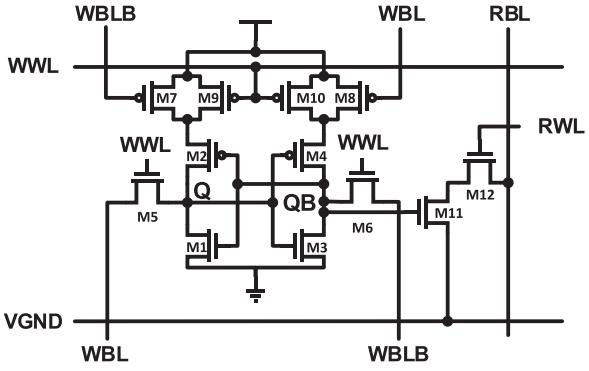


**Fig. 2.** The proposed 12T SRAM cell. Device M1 to M4 comprise back-to-back inverters. M5—M8 function as access transistors during write operation. M9 and M10 transfer power to inverters during holding data, while cutting during write operation. M11 decouples storage node QB from read bit line (RBL) as a conventional 8T SRAM cell, and M12 is an access transistor during read operation.

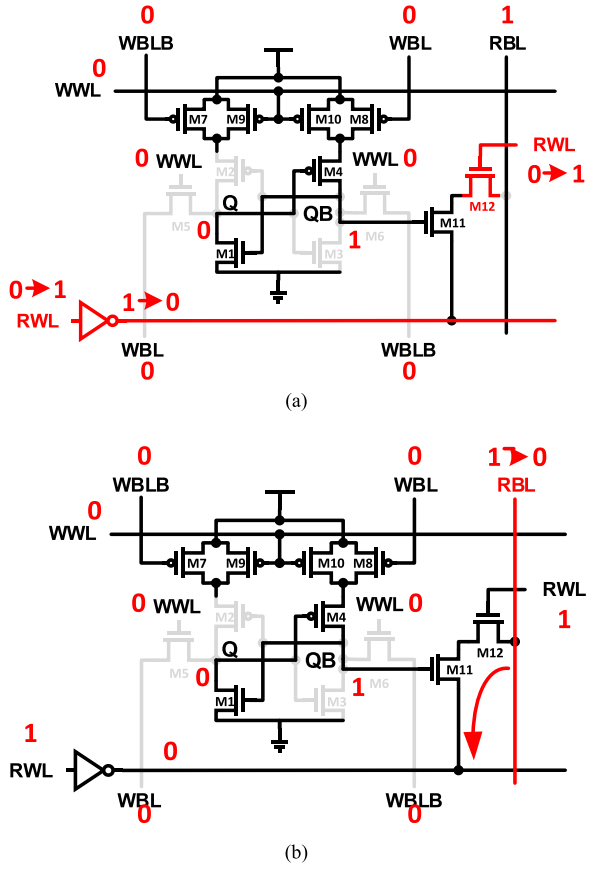


**Fig. 3.** Diagram of the proposed 12T SRAM during read operation. (a) When RWL asserted, the access transistor M12 is transparent, and VGND is driven to GND so that a path from RBL to GND is formed, depending on the value of node QB. (b) Pre-charged RBL is being discharged through M11 and M12, so nodes Q and QB can be evaluated.

#### 2.2.2. Write operation

The write operation is a key feature of the 12T SRAM cell design. Fig. 4 shows a series of processes in write operation. Device M5 to M10—six devices in total—are related to write operation. The basic principle is to make an SRAM cell operate in static mode without charge contention.

The write operation illustrated in Fig. 4 is writing '1' to node Q, assuming that '0' is initially stored at node Q and '1' is initially stored at node QB. To begin, keep '0' at node WBLB, while asserting '1' at node WBL so that M7 is turned on, and M8 is turned off, as shown in Fig. 4(a). Next, WWL is asserted, which causes M5 and M6 to turn on and M9 and M10 to turn off, as shown in Fig. 4(b). Notice that a path from the supply to node QB is cut, so that no current can flow into the storage nodes. Instead, a path from node QB to GND is formed. On the other side, a path from supply to node Q is formed through M5. Accordingly, discharge at node QB is incurred through M6, while charging Q through M5 as shown in Fig. 4(c). Please notice that there is

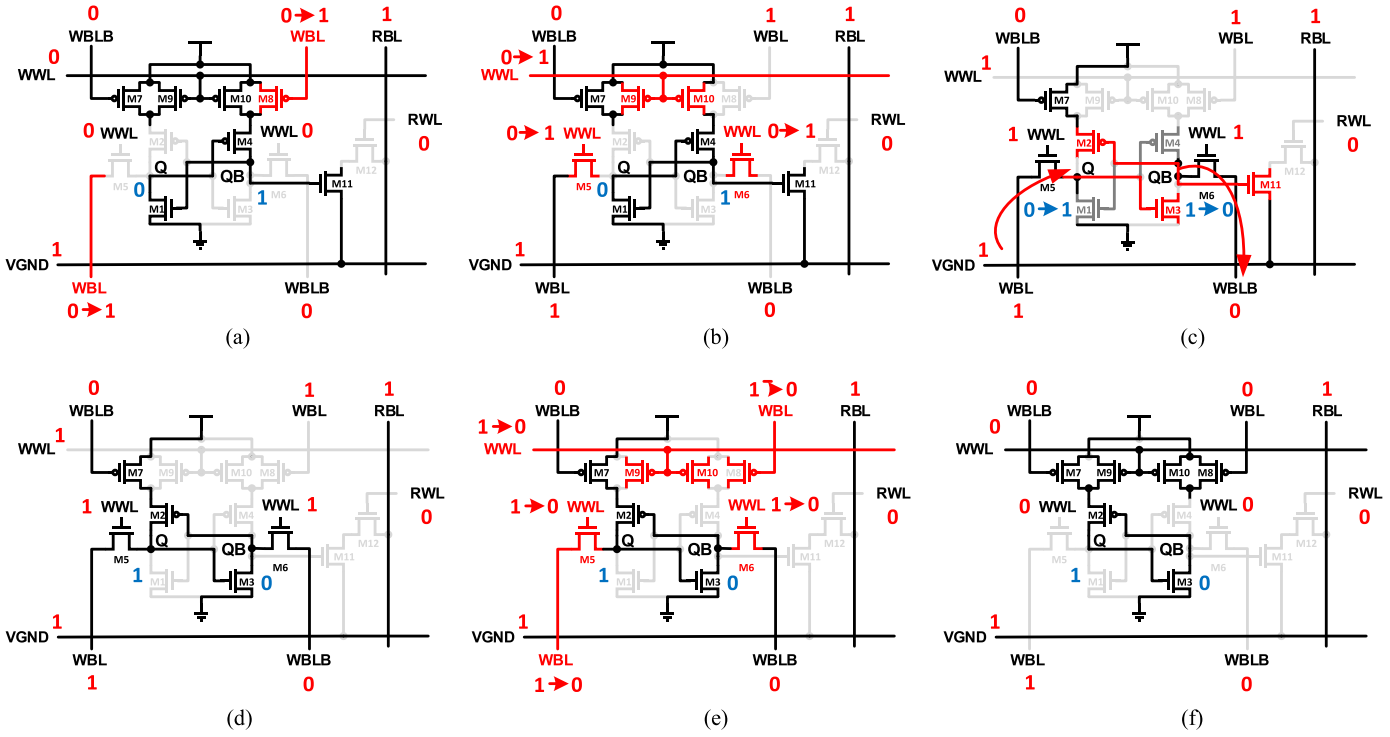


**Fig. 4.** A series of write operation process of the proposed 12T SRAM cell. This shows writing '1' to node Q storing '0' initially. (a) Assert '1' at WBL to write '1' to node Q, while keeping '0' at WBLB (M9 and M10 on. M8 and M11 off). (b) Assert $WL_{write}$ (M5 and M6 on. M7 off). This cuts power supply to inverters. (c) Discharge from node QB through M9 and M7 to GND (M2 on. M1 off). (d) Charge from VDD through M10 and M2 to node Q (M3 on. M4 off). (e) Reset WBL, WBLB, and $WL_{write}$ to finish write operation (M5, M6, M10, and M11 on. M7, M8, and M9 off). (f) Completion of write operation.

a charge contention between M1 and M5 (i.e. writing '1' at node Q). However, writing '0' at node QB would complete before writing '1' at node Q due to stronger $V_{GS}$ of M6 as well as no charge contention in discharging path. Thus, the initial charge contention between M1 and M5 would be eliminated after discharging the node QB. In other words, this process turns M2 on, while it turns M1 off, so that a path from VDD through M7 and M2 to node Q is transparent, while a path to GND is closed. This, in turn, helps charging node Q, causing M3 to become transparent, while switching M4 off as shown in Fig. 4(d). At this moment, writing '1' to node Q and '0' to node QB is completed. Subsequently, the asserted signal on WWL, WBL, and WBLB should be reset to '0' as shown in Fig. 4(e). With this reset, M7 through M10 can transfer power to the cross-coupled inverters, while M5 and M6 are turned off. Fig. 4(f) shows the state of the SRAM cell after the completion of write operation.

### 2.3. Sizing constraint

The proposed 12T SRAM cell has initial charge contention between the access transistor and the pull down transistor of one of the half cells during write operation. However, it will be eliminated when the write operation of the other half cell is complete, which means the write operation is sequentially conducted from one half cell to the other. Thus, sizing mostly affects the performance of an SRAM and its static and dynamic noise margins rather than its functionality. This is one of the advantages of the proposed 12T SRAM cell since engineering efforts to design an SRAM cell can dramatically be reduced. Unless performance is a matter of importance, every device size can be minimum. This can help to reduce energy consumption during read or write operation. For a balanced VTC, M2 and M4 can be sized twice as wide as M1 and M3. This makes pull-up and pull-down strength balanced, which causes the shape of each inverter's VTC as well as static noise margin. In addition, the proposed 12T bit cell does not have any feedback during read and write operations, so sizing M11 and M12 up could improve read performance as the conventional 8T bit cell. Moreover, sizing M5–M10 up can improve write performance since the sizes of M5 and M6 determine discharging time, while the sizes of M7 and M8 affect charging time. Thus, the proposed 12T bit cell can be designed according to any certain performance requirement without concerning either read upset or write upset.

## 3. Analytical model

In this section, an analytical model for write margin is proposed.

### 3.1. Read static noise margin

Fig. 5 shows static noise sources inserted at feedback nodes as in [30]. Since M7, M8, M9, and M10 are turned on, both nodes $V_1$ and $V_2$ are charged with VDD. In addition, M5 and M6 are also in off state. Only inverters (M1 through M4), M11 and M12 are relevant during the read operation. Accordingly, the proposed 12T SRAM cell is very similar to the conventional 8T SRAM cell during read operation, which

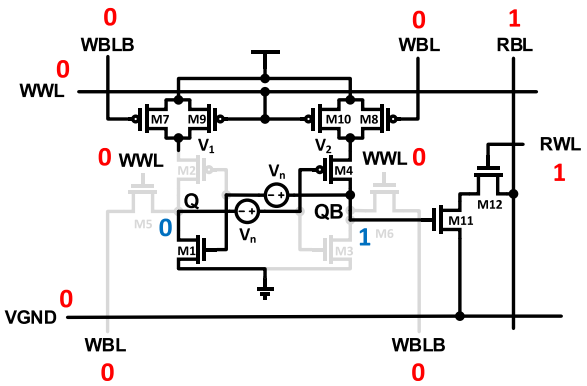


**Fig. 5.** Circuit diagram of 12T SRAM cell with static noise source $V_n$ inserted for read SNM.

will be shown in Section 4.

### 3.2. Definitions of write margin

Many definitions of write margin have been proposed in literature [31–34]. The conventional write static noise margin (WSNM) is based on the VTCs of the back-to-back inverters [31]. In this definition, two static noise sources are injected in the feedback loop of the back-to-back inverters so that these sources prevent the bit cell from writing. Accordingly, the minimum voltage of the noise sources that forces the bit cell to hold the previous data during write operation can be defined as WSNM. Another definition of write margin is bit line write margin (BLWM) [32]. In this definition, a static noise source is injected in a bit line which is supposed to be '0'. In other words, it can be assumed that a bit line driver cannot force a bit line to discharge fully. Since write operation begins with discharging, this injected noise source could affect the write operation, so BLWM can be the noise voltage at which discharging cannot flip the state of a bit cell. Other definitions of write margin are related to wordline [33,34]. In [33], the wordline voltage of a half cell is swept so that one of the inverters can flip at a certain voltage, from which to VDD can be a wordline write margin (WWM). In [34], a newly combined wordline write margin (CWWM) is proposed after analyzing the drawback of WWM. Instead of sweeping the wordline voltage of a half cell, the whole wordline voltage is swept in order to acquire CWWM. CWWM can be the difference between VDD and the wordline voltage where the storage nodes flip to the opposite state. These definitions are examined in [35], and it was concluded that CWWM follows PVT variations better than the others. However, WSNM would be used in analytical modeling since WSNM is a counterpart of the conventional read noise margin in write operation. Thus, it gives better understanding of the relations between each device.

### 3.3. Write static noise margin modeling

Static noise sources for write margin are inserted at feedback paths as shown in Fig. 6. In contrast with read SNM, the signs of noise sources are opposite since these sources should function to disturb write operation. In other words, these sources increase the stability of the SRAM cell during hold and read. Assume that state "1" is stored at node Q, and value "0" is being written, so WBLB is set as "1", while WBL as "0". In addition, WWL is also asserted, and RWL is deactivated (VGND is in "1" state). In this scenario, charges stored at node Q as well as at node $V_1$ begin to discharge through M5 since M2 is turned on. Accordingly, the voltage at node Q and at node $V_1$ is regarded as "0" in the dc analysis point of view. Moreover, the voltage at node $V_2$ can be considered VDD because M8 is always in 'on' state. Since the node voltage at Q is "0", writing "1" at QB is the completion of the write operation. Therefore, $V_n$ at which the drain current of M3 is the same as the one of M4 can be the static write margin since charges can barely be accumulated at QB, meaning almost "0" state. With these assumptions, the analytical model for write margin is acquired.

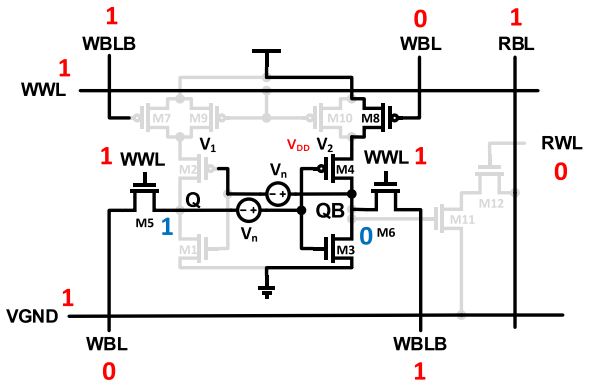


**Fig. 6.** Circuit diagram of 12T SRAM cell with static noise source $V_n$ injected for the conventional write static noise margin (WSNM).

#### 3.3.1. Super-threshold model

Assume M3 operates in the linear region, while M4 operates in the saturation region since "0" is stored at QB, so $V_{DS4}$ is almost VDD. Equating drain currents of both M3 and M4 results in:

$$\frac{k_4}{2}(V_{SG4} - V_{tp})^2 = k_3 V_{DS3}\left(V_{GS3} - V_{tn} - \frac{V_{DS3}}{2}\right) \tag{1}$$

where $k_3 = \mu_n C_{ox}(\frac{W}{L})_3$, $k_4 = \mu_p C_{ox}(\frac{W}{L})_4$, and $V_{tn}$ and $V_{tp}$ are the threshold voltages of nMOS and pMOS, respectively. For simplicity, $\mu_p$ and $V_{tp}$ are treated as positive values.

From Kirchhoff's voltage law (KVL), the following equations are acquired:

$$V_{GS3} = V_Q + V_n \tag{2}$$

$$V_{SG4} = V_{DD} - V_Q - V_n \tag{3}$$

$$V_Q = 0. \tag{4}$$

Notice that we only have the VTC of inverter 2; the VTC of inverter 1 is constant ($V_Q$=0). Substituting these into (1) yields:

$$V_{DS3}{}^2 - 2(V_n - V_{tn})V_{DS3} + \frac{\mu_p}{\mu_n}\beta(V_{DD} - V_{tp} - V_n)^2 = 0 \tag{5}$$

where $\beta = (\frac{W}{L})_4/(\frac{W}{L})_3$

When (5) has two distinct real roots, the SRAM cell is regarded as holding the current state—retaining bistability. If (5) has two distinct complex roots, the SRAM cell cannot hold data—monostable, so write operation can be performed. Therefore, $V_n$ at which (5) has a double root can be the write margin—both VTCs coincide at a point. This condition is identical to the discriminant of the quadratic Eq. (5) as shown below:

$$aV_{DS3}{}^2 + bV_{DS3} + c = 0 \tag{6}$$

or

$$b^2 = 4ac$$

$$b = -2\sqrt{ac} \ (\because b<0). \tag{7}$$

When (6) and (7) are applied to (5), the following equation is yielded:

$$2(V_n - V_{tn}) = 2\sqrt{\frac{\mu_p}{\mu_n}\beta}(V_{DD} - V_{tp} - V_n) \tag{8}$$

After solving (8) for $V_n$, the static write margin for the super-threshold operating condition can be acquired:

$$\therefore WM_{static,super-V_{th}} = \frac{V_{tn} + \sqrt{\frac{\mu_p}{\mu_n}\beta}(V_{DD} - V_{tp})}{1 + \sqrt{\frac{\mu_p}{\mu_n}\beta}}. \tag{9}$$

#### 3.3.2. Sub-threshold model

Sub-threshold modeling is similar to the super-threshold modeling except for the drain current expression. In this model, every parameter is treated as a positive value. At node QB, the drain currents of M3 and M4 can be equated by Kirchhoff's current law (KCL).

$$I_{SD4} = I_{DS3}. \tag{10}$$

The drain current of each device are represented below:

$$I_D = I_S e^{\frac{V_{GS}-V_t}{n\phi_T}}\left(1-e^{-\frac{V_{DS}}{\phi_T}}\right) \quad (11)$$

where $I_S = \mu(\frac{W}{L})\sqrt{\frac{q\epsilon_{Si}NDEP}{2\Phi_S}}(\phi_T)^3$, $n = 1+\frac{C_d}{C_{ox}}$, $\phi_T = \frac{kT}{q}$.

Since $1 \gg e^{-\frac{V_{DS}}{\phi_T}}$, $e^{-\frac{V_{DS}}{\phi_T}}$ term can be dismissed, so substituting (11) into (10) yields:

$$I_{S,4}e^{\frac{V_{SG4}-V_{tp}}{n\phi_T}} = I_{S,3}e^{\frac{V_{GS3}-V_{tn}}{n\phi_T}}. \quad (12)$$

As the case of super-threshold modeling, the same conditions—(2) to (4)—are applicable to (12). After substitution, solving (12) for $V_n$ yields the static write margin for sub-threshold condition:

$$\therefore WM_{static,sub-V_{th}} = \frac{1}{2}n\phi_T \ln\left(\frac{\mu_p}{\mu_n}\beta e^{\frac{V_{DD}-V_{thp}+V_{thn}}{n\phi_T}}\right). \quad (13)$$

## 4. Simulation results

### 4.1. Analytical model

WSNM analytical models developed in Section 3 are compared with simulation results as shown in Fig. 7.

Fig. 7 shows the comparison of super-threshold and sub-threshold models with simulation results versus VDD. The error range of super-threshold model is 3.1–8.7%, while sub-threshold model has 8.1–14.2% error range. The reason for greater error of the sub-threshold model is that leakage current exponentially increases as the device goes to deep sub-threshold region, and we assumed M1, M2, M7, and M9 were completely off in modeling, while they are not completely off due to sub-$V_{th}$ VDD.

### 4.2. Simulation setup

The proposed 12T cell was analyzed against the conventional 6T, 8T [11], and the 10T [26] cells. Sizing of each bit cell was determined as follows. The pull-up ratio (PR), which is defined as the ratio of the size of the pull up transistor to the size of the access transistor, of the 6T bit cell is set to 1, and the cell ratio (CR), the ratio of the size of the pull down transistor to the size of the access transistor, is set to 2. Both PR and CR of the 8T bit cell is set to 1, and the read access transistors are sized as minimum. All devices of the 10T and the proposed 12T bit cell are sized as minimum. All experiments were conducted with these setups. The operating supply voltage is set as a near-threshold voltage

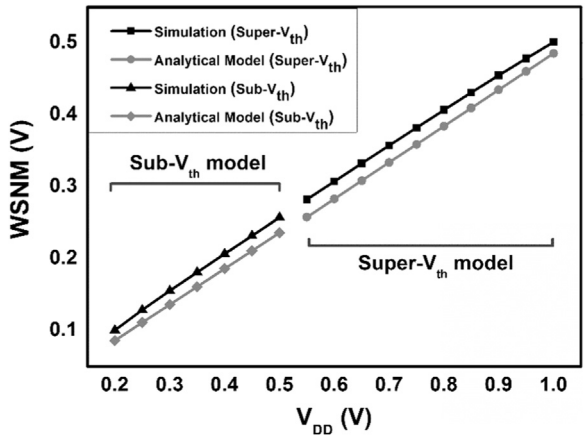


**Fig. 7.** Comparison of the analytical model with simulation results versus $V_{DD}$ with β=2. The error ranges of super-$V_{th}$ and sub-$V_{th}$ are from 3.1–8.7% and 8.1–14.2%, respectively.

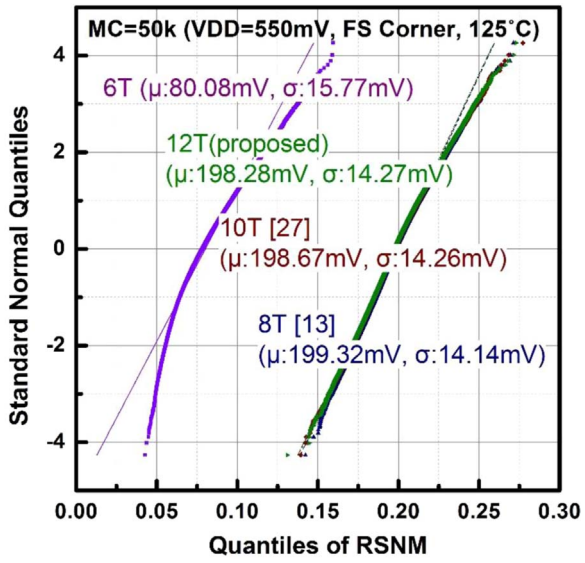


**Fig. 8.** 50,000 RSNM Monte-Carlo simulation results for 6T, 8T [13], 10T [27], and the proposed 12T SRAM cells in 40 nm CMOS technology. At VDD=550 mV, the RSNMs of 6T, 8T, 10T, and 12T are 80.08 mV, 199.32 mV, 198.67 mV, and 198.28 mV, respectively. The RSNM of the proposed 12T SRAM cell is comparable with 8T and 10T bit cells.

(i.e. 550 mV) since it provides a certain amount of performance, while saving energy much.

### 4.3. Read static noise margin

50k Monte-Carlo pre-layout schematic simulation results of RSNM at VDD=550 mV, FS corner, and 125 °C is shown in Fig. 8. The RSNMs of 6T, 8T, 10T, and 12T bit cells are 80.08 mV, 199.32 mV, 198.67 mV, and 198.28 mV, respectively. According to the distributions, all bit cells can be considered robust under ± 6σ local process and mismatch variations. In addition, the RSNM of the proposed 12T bit cell is comparable to the conventional 8T bit cell and the 10T bit cell, while the conventional 6T bit cell is more vulnerable than the others.

### 4.4. Static write margin

Since noise can incur at any node including a storage node, wordline, and bit line, investigation of each write margin definition is essential. 50,000 WSNM Monte-Carlo pre-layout bitcell level simulation results at VDD=550 mV, SF corner, and −30 °C under process and mismatch variations are shown in Fig. 9. The curves of the 10T and the proposed 12T bit cell resemble the ideal shape shown in Fig. 1. Notice that the VTC of a half cell is a straight line along with y-axis even under process and mismatch variations. This is because a feedback loop is cut in the 10T and the 12T bit cell during write operation. Thus, the proposed bit cell provides mono stability even though the VTC of the other half cell is fluctuating under process and mismatch variations.

The statistical distributions of write margin simulation results are shown in Fig. 10. The 6 T and 8 T bit cells fail in some iterations of CWWM, and BLWM, while the 10T and the 12T bit cell do not fail at all in any write margin definition.

The mean of WSNM for 6T, 8T, 10T, and 12T bit cells are 173.1 mV, 186.4 mV, 305.6 mV, and 307.8 mV, respectively. According to the distributions, 6T and 8T are robust under ± 4σ variations, while 10T and 12T are robust under more than ± 12σ variations, which can be concluded by the extrapolation of the distributions. The mean of CWWM for 6T, 8T, 10T, and 12T are 44.9 mV, 54.8 mV, 317.1 mV, and 251.5 mV, respectively. Note that the conventional 6T and 8T bit cells fail 5816 and 3856 times, respectively. In BLWM, the mean of 6T, 8T, 10T and 12T are

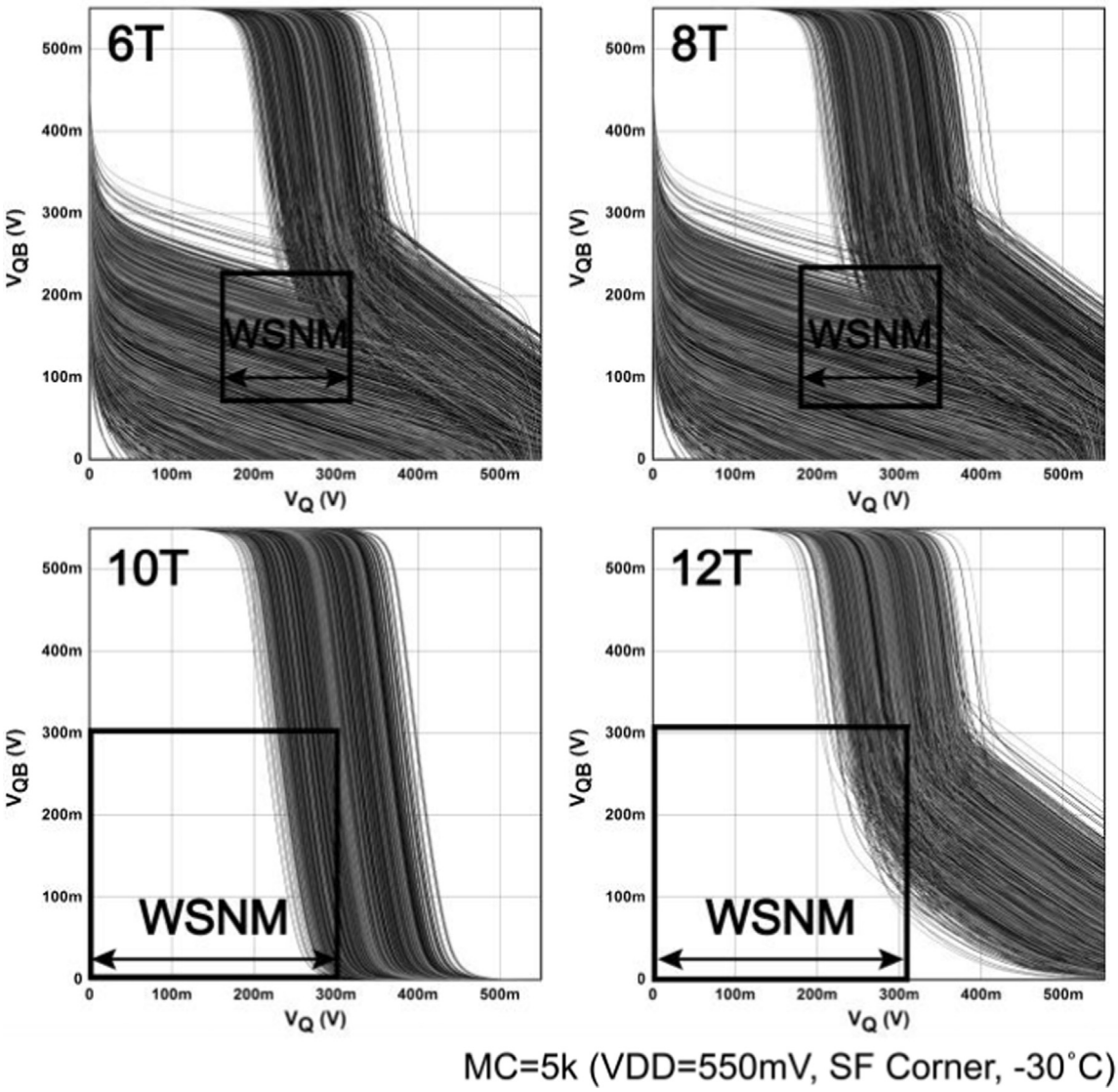


**Fig. 9.** 5,000 WSNM Monte-Carlo simulation results for 6T, 8T, 10T, and 12T SRAM cells at VDD=550 mV, SF corner, and −30 °C. The curves of the 10T and the proposed 12T bit cell are close to the ideal case (see Fig. 1), so that they are more mono-stable than those in 6T and 8T bit cell under process and mismatch variations.

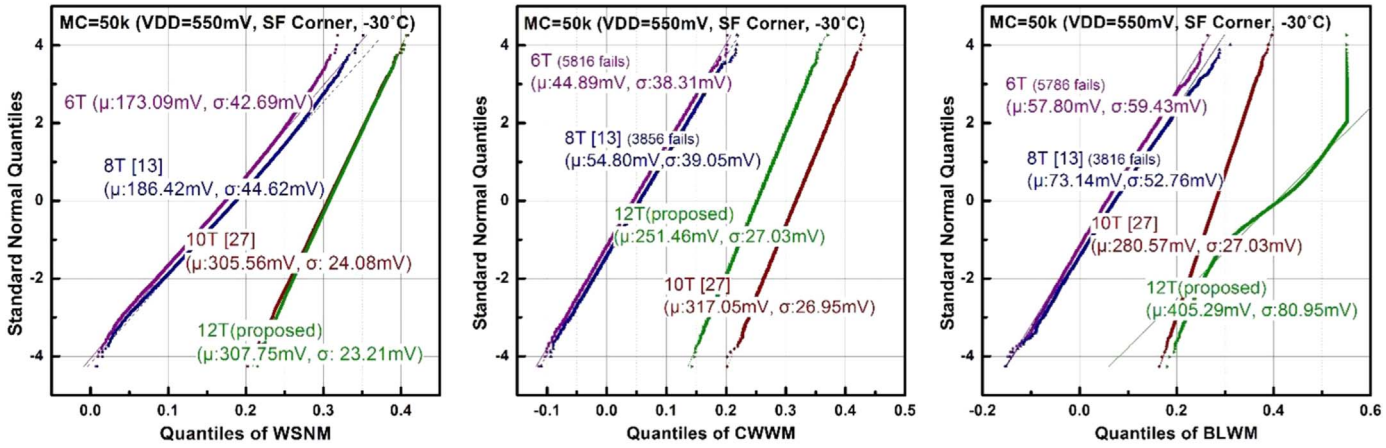


**Fig. 10.** WSNM, CWWM, and BLWM 50,000 Monte-Carlo simulation statistical distributions for 6T, 8T, 10T, and 12T SRAM cells at VDD=550 mV, SF corner, −30 °C. The μ/σ of WSNM for 6T, 8T, and 12T are 2.24, 2.36, and 4.95, respectively. The μ/σ of BLWM for 6T, 8T, and 12T are 1.34, 1.51, and 15.15, respectively. The μ/σ of CWWM for 6T, 8T, and 12T are 1.60, 1.78, and 4.65, respectively. Note that those statistics in WSNM exclude failed results, so the μ/σ of 6T and 8T bit cells should be worse when including those failed results.

**Table 1**
Write Margin Simulation Results (50,000 MC, SF corner, T=−30 °C).

| | | 6T | 8T[13] | 10T[27] | 12T (proposed) |
|---|---|---|---|---|---|
| **WSNM** | **μ** | 173.1 mV | 186.4 mV | 305.6 mV | 307.8 mV |
| | **σ** | 42.7 mV | 44.6 mV | 24.1 mV | 23.2 mV |
| | **fail** | **No fail** | **No fail** | **No fail** | **No fail** |
| **CWWM** | **μ** | 44.9 mV | 54.8 mV | 317.1 mV | 251.5 mV |
| | **σ** | 38.3 mV | 39.1 mV | 27.0 mV | 27.0 mV |
| | **fail** | **5816 fails** | **3856 fails** | **No fail** | **No fail** |
| **BLWM** | **μ** | 57.8 mV | 73.1 mV | 280.6 mV | 405.3 mV |
| | **σ** | 49.4 mV | 52.8 mV | 27.0 mV | 81.0 mV |
| | **fail** | **5786 fails** | **3816 fails** | **No fail** | **No fail** |

57.8 mV, 73.1 mV, 280.6 mV and 405.3 mV, respectively. The 6T and 8T bit cells also fail 5786 and 3816 times, respectively. The statistics of the write margin simulations are shown in Table 1. As shown in the table, the proposed bit cell has more BLWM than the compared 10T bit cell, while it has less CWWM. The reason why the 10 T cell has more CWWM is that the 10T cell cuts a feedback path by weakening both a PMOS and an NMOS, while the proposed bit cell cuts the feedback only by a PMOS. Thus, the 10T cell can weaken the feedback more with the same amount of wordline voltage applied. The reason why the proposed bit cell has more BLWM is that data is written by both BL and BLB, while the 10T cell is only driven by a bit line. As shown in the figure and the table, we can conclude that the proposed 12T SRAM bit cell is robust under ± 6σ variations at VDD=550 mV, SF corner, and −30 °C by extrapolation.

### 4.5. Dynamic write margin

Dynamic noise margin for a write operation (DNM) is analyzed for 6T, 8T, 10T, and 12T. Among the previously proposed DNM's, the minimum width of the WL assertion pulse to make a bitcell reach to the switching threshold [36] is used for this analysis. The simulation setting is shown in Fig. 11. A bitwise column consists of 128 bitcells, and a wire RC model is inserted on the bitline. 50,000 Monte-Carlo simulation was conducted at VDD=550 mV, SF corner, and −30 °C. DNM per iteration is found by sweeping wordline width.

The simulation results are shown in Fig. 12. The proposed 12T bit cell did not incur any failure, while the other cells did. The mean of

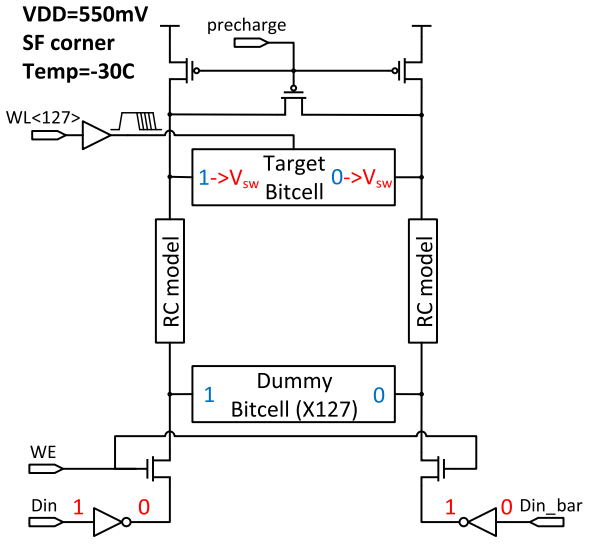


**Fig. 11.** Dynamic write noise margin simulation setting. 128 cells share a bitline, and a wire RC model is inserted on a bitline. The minimum width of wordline to be able to make the target cell switch is found by sweeping the wordline assertion pulse width.

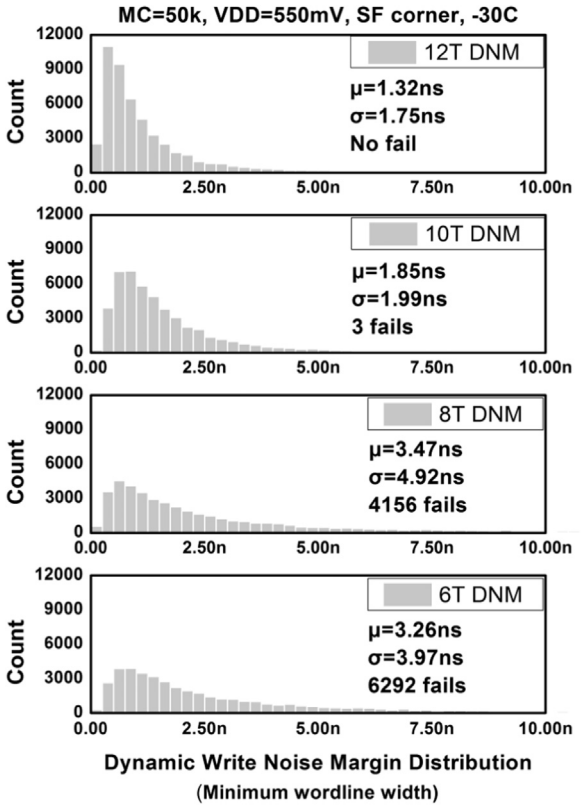


**Fig. 12.** 50,000 Monte-Carlo DNM simulation results for 6T, 8T [13], 10T [27], and the proposed 12T SRAM cells in 40 nm CMOS technology. At VDD=550 mV, the proposed bit cell has more DNM than the other compared cells. In addition, it does not fail during 50,000 iterations, while 6T, 8T, and 10T cell fails 6,292, 4,156, and 3 times, respectively.

DNM for 6T, 8T, 10T, and 12T are 3.26 ns, 3.47 ns, 1.85 ns, and 1.32 ns, respectively. The standard deviations of DNM for 6T, 8T, 10T, and 12T are 3.97 ns, 4.92 ns, 1.99 ns, and 1.75 ns. Note that the mean values exclude failed interations, so these numbers show a DNM tendency. In conclusion, the proposed 12T cell is dynamically more stable than the other compared cells.

### 4.6. Leakage current

One of important metrics of an SRAM bit cell is the total bit cell leakage current since it limits the number of cells sharing bit lines. The total bit cell leakage of the 6T, 8T, 10T, and 12T at VDD=550 mV, TT corner, 25 °C are 6.42 nA, 5.04 nA, 3.94 nA and 4.12 nA, respectively. This is reasonable since the 10T cell has a single bitline, and both 10T and 12T cells have more stacks than 6T and 8T cells.

### 4.7. Performance

Read access time of a column of 128 bit cell is simulated as the delay from 50% of read wordline voltage to 100 mV voltage difference

**Table 2**
SRAM Cell Delay Comparison (VDD=0.55 V).

| SRAM bit cell | Read (FS, 125 C) | Write (SF, −30C) |
|---|---|---|
| 6 T | 22.07 ps | 2.45 ns |
| 8 T | 26.65 ps | 2.19 ns |
| 10 T | 29.28 ps | 1.73 ns |
| 12 T | 29.89 ps | 1.28 ns |

Write delay is simulated from 50% of wordline voltage to 50% of the storage node voltage, while read delay from 50% of wordline voltage until when the voltage difference between bitline and bitline bar to be 100 mV.

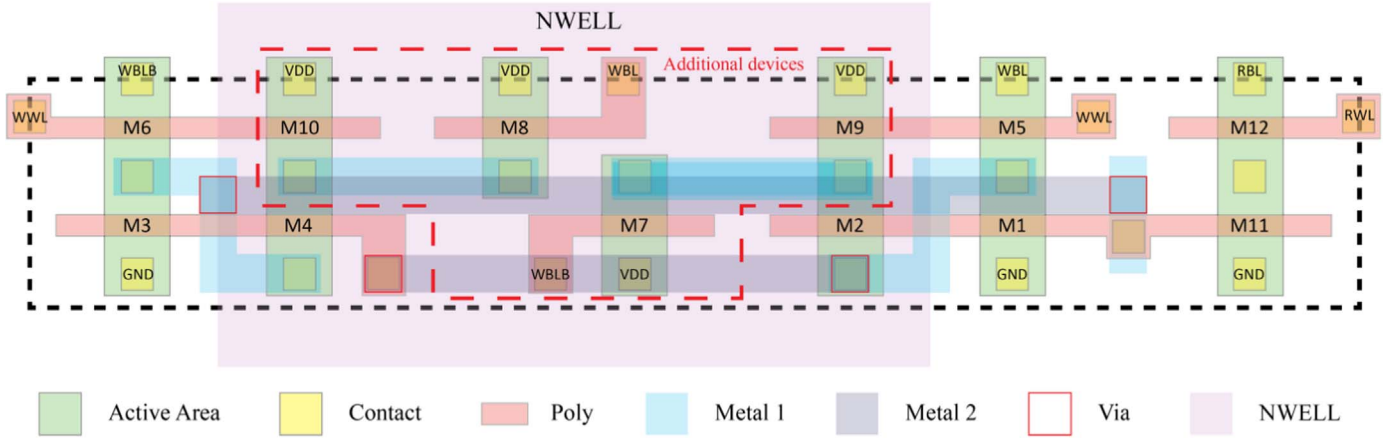


**Fig. 13.** The stick diagram of the proposed 12T bit cell. It is 2-poly pitch height as the conventional 6T and 8T cells, but can only share three sides (top, left, and right). Thus, the height of the proposed cell is 1.18 times greater than the other two cells. In addition, the width of the proposed cell is 1.65 times and 1.46 times greater than the 6T and 8T cells, respectively. Overall, the area overhead is 1.96 times and 1.74 times greater than the 6T and 8T cells, respectively.

**Table 3**
SRAM Cell Area Comparison.

| SRAM bit cell | Number of bitlines | Area (with respect to 8 T) |
|---|---|---|
| 6 T | 2 BL | 0.77× |
| 8 T[13] | 2 WBL/1 RBL | 1× |
| 8 T[16] | 2 WBL/1 RBL | 1.2× |
| 10 T[19] | 2 WBL/1 RBL | 1.6× |
| 10 T[20] | 2 WBL/1 RBL | 1.6× |
| 10 T[21] | 2 BL | 1.6× |
| 9 T[26] | 2 WBL/2 RBL | 1.4× |
| 12 T (This work) | 2 WBL/1 RBL | 1.7× |

between BL and BLB (or a reference dummy bitline). Simlarly, write access time is simulated as the delay from 50% of write wordline voltage to 50% of written storage node voltage in the 128-bitcell column array. The simulation results are shown in Table 2.

In read operation, the proposed bit cell shows a comparable performance to the 10T bit cell. The reason why 8T has a better delay than 10T and the proposed 12T is that both 10T and 12T cells have an additional stack on pull-up network, so that the bitcells can't quickly recover voltage droop due to leakage. This weakens the drivability of the read port transistor. The conventional 6T bitcell shows the best performance in reading since it has a differential read port in additional to that the 6T cell has a greater CR than 8T, 10T and 12T cells (i.e. CR=2). If the read access transistor of 8T, 10T and 12T cells are sized up, the read performance can be improved, but it would trade power and area off.

For write operation, the proposed 12T bit cell shows the best result. This is because the proposed 12T cell does not have a feed back for overdriving in a discharging path. 10T cell also shows a good performance for writing since it also cuts a feedback during write. However, it has a single write port, so the performance is worse than the proposed 12T cell. The conventional 6T SRAM cell gives the worst write delay due to a higher CR.

In conclusion, the prospoed 12T bit cell provides comparable performance with the conventional 6T and 8T [11], and the 10T [26] SRAM cells. When there is a certain requirement of performance, the proposed 12T bit cell could achieve the requirement since there is no sizing constraint both in read and write operations. In this case, area and power can be traded off with performance.

### 4.8. Cell area

The layout of the proposed 12T bit cell is shown in Fig. 13. The layout is 2-poly pitch height as in the conventional 6T and 8T cell layout, but only three sides (top, left and right) can be shared because the source terminals of M2 and M4 are not connected to VDD (i.e. the conventional 6T and 8T cell layout shares this terminal to another cell so that the bit cell area can drastically be reduce). Thus, the height of the proposed bit cell is 1.18 times greater than the other two cells which can share contacts with other cells both at the top and at the bottom. In addition, the width of the proposed cell is 1.65 times and 1.46 times greater than the 6T and 8T cells, respectively. Since the source terminals of M2 and M4 should be shared with four additional devices (M7 through M10), the drain terminals of inverters are connected by twisted metal 1 layer. Please note that the devices in the area lineated with read dot lines are additional ones compared to the conventional 8T bit cell. Overall, the area overhead of the proposed bit cell is 1.96 times and 1.74 times greater than 6T and 8T cells, respectively. The cell area comparison with respect to the conventional 8T cell is shown in Table 3. Although the proposed 12T cell has 2 or 3 more transistors than the previous proposed bit cells, the cell area overhead is not too great thanks to the layout optimization.

## 5. Conclusions

The proposed 12T bit cell dramatically improves the write margin by eliminating the charge contention due to the feedback structure of an SRAM cell. Its innate structure allows reliable operation during writing by blocking the power supply route. Since there is no charge contention, no sizing constraint exists. In order to improve RSNM, pull-up devices can be sized two times more than the pull-down devices for balancing the VTCs of back-to-back inverters. In addition, any device can be sized according to a certain performance requirement since there is no sizing constraint in the proposed structure. The VTC of the proposed cell in WSNM is very similar to the ideal curves suggested in Section 1 due to the feedback free structure during write. In three different definitions of write margin including WSNM, CWMM, and BLWM, the 12T cell is more robust than the conventional 6T and 8T cells, and it is comparable to the 10T cell [26]. In addition, the proposed 12T cell is more dynamically stable than the 6T, 8T, and 10T cells. Therefore, the proposed cell achieves a higher WSNM, BLNM, and DNM without sacrificing RSNM. Accordingly, the proposed 12T cell can be used for ultra-low power applications which requires low-voltage operations while demanding relatively low capacity since the area of memory block is comparable to the area of peripheral circuitry. In addition, the WSNM analytical model of the 12T cell is proposed. The super-threshold model fits within 8.7% errors, while the sub-threshold model fits within 14.2% errors. When β ratio changes from 1 to 5, the super-threshold model fits within 6.17%, while the sub-threshold model fits within 15.42% errors.

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